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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,338	12/31/2003	Peter N. Martin	42P17996	4703

7590 04/12/2006

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,338	MARTIN ET AL.	
	Examiner	Art Unit	
	Brian T. Misiura	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-13 and 15-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4, 5, 7, 8, 12, 13, 15, 16* is/are allowed.

6)☐ Claim(s) *1-3,9-11,17-20,22,23 and 25-36* is/are rejected.

7)☒ Claim(s) *21 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 3, 9, 10, 11, 17, 18, 19, 31, 32, and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by "PCI Standard Hot-Plug Controller and Subsystem Specification", Revision 1.0, dated June 20, 2001.

2. Reference, by "PCI Standard Hot-Plug Controller and Subsystem Specification", Revision 1.0, dated June 20, 2001, will be referred to as SHPC Spec for the remainder of the office action.

3. Per claim 1, SHPC Spec discloses: an apparatus, comprising:

- a hot-plug controller, the hot-plug controller having a blinking pattern controller to receive at least one command, the blinking pattern controller to (page 20, particularly, "Hot-plug system software has exclusive control of the indicator states by issuing commands to the SHPC."):
- cause execution of a blinking pattern on at least one indicator associated with at least one target peripheral component interconnect slot on a peripheral component interconnect bus (page 20),
- the blinking pattern being unique to the command being processed, wherein a first unique blinking pattern is to indicate a first command to turn the indicator "on" solid (pages 20-22, particularly, either "Power Indicator On" or "Attention Indicator On").

4. Per claim 3, SHPC Spec discloses: the apparatus of claim 1, wherein a second unique blinking pattern is to indicate a second command to apply power only to at least one target peripheral component interconnect slot (page 22, particularly, "When the Power Indicator is blinking, it means that the slot is powering up or powering down").

5. Per claims 9 and 17, SHPC Spec discloses: a method, comprising:

- receiving a command at a standard hot-plug controller from a microprocessor (page 20, particularly, "Hot-plug system software has exclusive control of the indicator states by issuing commands to the SHPC.");
- and causing execution of a blinking pattern on at least one indicator associated with at least one target peripheral component interconnect slot on a peripheral component interconnect bus (page 20),
- the blinking pattern indicating the command being processed (pages 20-22, particularly, either "Power Indicator On" or "Attention Indicator On"),
- the blinking pattern having a duty cycle that is less than or greater than approximately fifty percent (page 20, particularly, "Blinking indicators operate at a frequency of 1 to 2 Hz and 50% (+/-5%) duty cycle.).

6. Per claim 10 and 18, SHPC Spec discloses: the method of claim 9, further comprising receiving a command to turn the indicator "on," "off," or make the diode blink in a blinking pattern having a duty cycle of approximately fifty percent (page 20, particularly, "Blinking indicators operate at a frequency of 1 to 2 Hz and 50% (+/-5%) duty cycle.).

7. Per claim 11 and 19, SHPC Spec discloses: the method of claim 9, further comprising receiving a command to apply power to the target peripheral component interconnect slot (page 22, particularly, "When the Power Indicator is blinking, it means that the slot is powering up or powering down"), to enable the target peripheral component interconnect slot, to disable the target peripheral component interconnect

slot, or to change the speed of the peripheral component interconnect bus.

8. Per claim 31, SHPC Spec discloses: a method, comprising:

- receiving a command at a standard hot-plug controller from a microprocessor (page 20, particularly, "Hot-plug system software has exclusive control of the indicator states by issuing commands to the SHPC."); and
- causing execution of a blinking pattern on at least one indicator associated with at least one target peripheral component interconnect slot on a peripheral component interconnect bus (page 20),
- the blinking pattern indicating the command being processed (page 22, section "Power Indicator Blinking", indicates the slot is powering up or powering down).

9. Per claim 32, SHPC Spec discloses: the method of claim 31, further comprising receiving a command to turn the indicator "on," "off," or make the diode blink in a pattern having a duty cycle of approximately fifty percent (page 20, particularly, "Blinking indicators operate at a frequency of 1 to 2 Hz and 50% (+/-5%) duty cycle.).

10. Per claim 33, SHPC Spec discloses: the method of claim 31, further comprising receiving a command to apply power to the target peripheral component interconnect slot (page 22, particularly, "When the Power Indicator is blinking, it means that the slot is powering up or powering down")

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 2, 25, 26, 27, 28, 29, 30, 34, 35, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over "PCI Standard Hot-Plug Controller and Subsystem Specification", Revision 1.0, dated June 20, 2001 in view of "PCI Express to PCI/PCI-X Bridge Specification", Revision 1.0, dated July 14, 2003.

12. Per claim 2, SHPC Spec discloses: the apparatus of claim 1,

- wherein a second unique blinking pattern is to indicate a second command to turn the indicator "off," (pages 20-22, particularly, either "Attention Indicator Off" or "Power Indicator Off)
- or wherein a third unique blinking pattern is to indicate a third command to make the diode blink in a blinking pattern having a duty cycle of approximately fifty percent (page 20, particularly, "Blinking indicators operate at a frequency of 1 to 2 Hz and 50% (+/-5%) duty cycle.)

SHPC Spec does not disclose: the PCI bus being a PCI-Express bus.

However, PCI-E Bridge Spec discloses: wherein the peripheral component interconnect bus comprises a PCI-Express bus (page 21, figure 1-1).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of PCI-E Bridge Spec into the system of SHPC Spec in order to benefit from the improvements and new capabilities that the PCI-Express bus holds over the standard PCI bus configuration.

13. Per claims 25 and 28, SHPC Spec discloses: a system, comprising:

- a peripheral component interconnect bus having at least one peripheral component interconnect slot thereon (page 19, particularly, "A standard usage model allows customers to use the PCI hot-plug slots on all of their systems without having to retrain operators."),
- the peripheral component interconnect slot having at least one indicator associated therewith (page 20, table 2-1),
- the hot-plug controller to receive a command (page 20, particularly, "Hot-plug system software has exclusive control of the indicator states by issuing commands to the SHPC."):,
- and cause execution of a blinking pattern on at least one indicator (page 20),
- the blinking pattern to indicate (the command being processed) (pages 20-22, particularly, either sections "Power Indicator On" or "Attention Indicator On"), (an error occurring during processing of the command) (page 21, "Attention Indicator On" section)
- the blinking pattern having a duty cycle that is less than or greater than approximately fifty percent (page 20, particularly, "Blinking indicators operate at a frequency of 1 to 2 Hz and 50% (+/-5%) duty cycle.).

SHPC Spec does not disclose: a bridge coupled to the peripheral component interconnect bus, the bridge having a hot-plug controller coupled to the peripheral component interconnect bus.

However, PCI-E Bridge Spec discloses: a bridge coupled to the peripheral component interconnect bus, the bridge having a hot-plug controller coupled to the peripheral component interconnect bus (page 25, section 1.3.3. "Optional Capabilities),

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of SHPC Spec into the system of PCI-E Bridge Spec to incorporate error detection and forwarding between interfaces.

14. Per claims 26 and 29, PCI-E Bridge Spec discloses: further comprising a memory coupled to the bridge (Bridge spec, page 21, figure 1-1), which is not disclosed by SHPC Spec.

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of SHPC Spec into the system of PCI-E Bridge Spec it is standard for a memory to be coupled to a PCI-E Bridge.

115. Per claims 27 and 30, PCI-E Bridge Spec discloses: wherein the memory is a static random access memory (SRAM), (page 87, section 5.1.1.3., this specification describes use of caching, which is often implemented using fast static memory such as SRAM).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of SHPC Spec into the system of PCI-E Bridge Spec to implement a cache in the SHPC system for optimizing memory read time.

16. Per claim 34, SHPC Spec discloses: a system, comprising: a chipset including:

- a hot-plug controller having a blinking pattern controller to receive at least one command (page 20, particularly, "Hot-plug system software has exclusive control of the indicator states by issuing commands to the SHPC.");,
- the blinking pattern controller to cause execution of a blinking pattern on at least one indicator associated with at least one target peripheral component interconnect slot on a peripheral component interconnect bus,
- the blinking pattern being unique to the command being processed, wherein a first unique blinking pattern is to indicate a first command to turn the indicator "on" solid (pages 20-22, particularly, either "Power Indicator On" or "Attention Indicator On"),

SHPC Spec does not disclose: an SRAM coupled to the hot-plug controller.

However, PCI-E Bridge Spec discloses: static random access memory (SRAM) coupled to the hot-plug controller), (Bridge Spec, page 87, section 5.1.1.3., this specification describes use of caching, which is often implemented using fast static memory such as SRAM).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of SHPC Spec into the system of PCI-E Bridge Spec to implement a cache in the SHPC system for optimizing memory read time.

17. Per claim 35, SHPC Spec discloses: the system of claim 34, wherein a second unique blinking pattern is to indicate a second command to apply power to the target peripheral component slot (page 22, section "Power Indicator Blinking", means the slot is powering up).

18. Per claim 36, SHPC Spec discloses: the system of claim 34, wherein a second unique blinking pattern is to indicate a second command to disable the target peripheral component interconnect slot (page 22, section "Power Indicator Blinking", means the slot is powering down, which can also be interpreted as moving to an enabled state).

19. Claims 20, 22, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over "PCI Standard Hot-Plug Controller and Subsystem Specification", Revision 1.0, dated June 20, 2001 in view of Juntunen et al, U.S. Patent No. 6,772,018.

20. Per claim 20, SHPC Spec discloses: an article of manufacture including a machine-accessible tangible storage medium having data that, when accessed by a machine, cause the machine to perform the operations comprising:

- receiving at least one command at a standard hot-plug controller from a microprocessor (page 20, particularly, "Hot-plug system software has exclusive control of the indicator states by issuing commands to the SHPC."); and
- causing execution of unique blinking patterns on at least one indicator associated with at least one target peripheral component interconnect slot on a peripheral component interconnect bus (page 20),

SHPC Spec does not disclose: the unique blinking pattern indicating unique errors.

However, Juntunen discloses: unique blinking patterns indicating unique errors occurring during processing of the command (column 10 lines 29-67, figure 4 numerals 113, 159, 107, 115).

- It would have been obvious to one having ordinary skill in the art at the time of the applicant's claimed invention to incorporate the teaching of Juntunen into the system of SHPC Spec in order to display different commands with only one indicator.

21. Per claim 22, SHPC Spec discloses: the article of manufacture of claim 20, wherein the machine-accessible tangible storage medium further includes data that cause the machine to perform operations comprising causing execution of the blinking pattern at a duty cycle that is less than or greater than approximately fifty percent (page 20, particularly, "Blinking indicators operate at a frequency of 1 to 2 Hz and 50% (+/-5%) duty cycle.).

22. Per claim 23, SHPC Spec discloses: the article of manufacture of claim 20, wherein the machine-accessible tangible storage medium further includes data that cause the machine to perform operations comprising indicating an error occurring after power is applied to the target slot (page 21, section "Attention Indicator On", particularly, "Examples of operation problems include problems related to power faults.", which would occur after power was already applied to the slot.)

Allowable Subject Matter

23. Claims 4, 5, 7, 8, 12, 13, 15, and 16 are allowed.

24. Claims 21 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

25. The following is a statement of reasons for the indication of allowable subject matter:

26. Claims 4 and 12 are considered to be containing allowable subject matter, primarily due to the fact that they both claim "a first unique blinking pattern to indicate a

hard error occurring during processing of a command and a second unique blinking pattern to indicate a soft error occurring during processing of a command."

27. Claims 5, 7, 8, 13, 15, and 16 inherit the allowable subject matter of Claims 4 and 12.

Response to Amendment

23. The examiner respectfully withdraws the rejection of Claims 8-10, 16-18, 22, 25-26, and 28-29 under 35 U.S.C. 112, Second Paragraph due to applicants' adding claim language "tangible storage".

24. In view of the applicants' amended claims, the examiner respectfully withdraws the rejection of claims 17-24 under 35 U.S.C. 101.

25. Applicant's arguments with respect to claims 1-5, 7-13, and 17-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian T. Misiura whose telephone number is (571) 272-0889. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571)272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Misiura
3/29/2006

JOHN R. COTTINGHAM
PRIMARY EXAMINER